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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/802,234	03/08/2001	Kirk Prall	MIO 0065 PA	6679

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EXAMINER

QUINTO, KEVIN V

ART UNIT	PAPER NUMBER
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2826

DATE MAILED: 12/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Applicant(s)

09/802,234

Applicant(s)

PRALL, KIRK

Examiner

Kevin Quinto

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 01 October 2002.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-36 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-9, 15, 16, 20, 21, 24, 25 and 29-33 is/are allowed.
- 6) ☒ Claim(s) 10-14, 17-19, 22, 23, 26-28 and 34-36 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Claim Rejections - 35 USC § 112***

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 23, and 34-36 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claim 23 contains the limitation "a self aligned floating gate formed over the n-type layer." However claim 23 contains a first n-type layer and a second n-type layer. It is unclear to the examiner as to which n-type layer is being referred to in the limitation "a self aligned floating gate formed over the n-type layer."

4. Claim 34 recites the limitation "the drain" in the first line of the claim. There is insufficient antecedent basis for this limitation in the claim.

5. Claims 35 and 36 recite the limitation "the floating gate" in the first line of each of these claims. There is insufficient antecedent basis for this limitation in the claim.

### ***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

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7. Claims 10-14, 17-19, 22, and 26-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Hofmann et al. (USPN 5,998,261).

8. In reference to claim 10, Hofmann et al. (USPN 5,998,261, hereinafter referred to as the "Hofmann" reference) discloses a similar device. Figure 5 of Hofmann illustrates a memory cell with a first transistor having a source (14a), a drain (14b), and a gate (11). There is a select transistor coupled to the first transistor having a source (14a), a drain (14b), and a gate (13). Figure 6 shows that the select transistor gate (13a) is substantially perpendicular to the first transistor gate (11). The cell area is  $2F^2$  (column 6, lines 15-19); which is less than  $4.5F^2$ .

9. With regard to claim 11, the upper surface of the source (14a) of the first transistor is located below the lower surface of the drain (14b) of the first transistor.

10. In reference to claim 12, the source (14a) and drain (14b) of the first transistor are shared as the source (14a) and drain (14b) of the select transistor.

11. With regard to claim 13, Hofmann (USPN 5,998,261) discloses a similar device. Figure 5 of Hofmann illustrates a memory device with a p-type layer (3) over a first n-type layer (14a). There is a second n-type layer (14b) formed over the p-type layer (3). It is understood that a vertical channel is formed in the p-type layer (3). The memory cell area is  $2F^2$  (column 6, lines 15-19); which is less than  $4F^2$ .

12. In reference to claim 14, the first n-type layer (14a) forms a buried source and the second n-type layer (14b) forms a drain.

13. With regard to claims 17 and 18, Hofmann (USPN 5,998,261) discloses a similar device. Figure 5 of Hofmann illustrates a memory device with a buried source (14a) formed over a substrate (1). It is understood that a vertical channel is formed over the buried source (14a). A

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drain (14b) is over the vertical channel. The memory cell area is  $2F^2$  (column 6, lines 15-19); which is less than  $4F^2$ . The examiner notes that the applicant has also claimed that the "vertical channel is formed using epitaxial deposition." This language places claims 17 and 18 into the form of product-by-process claims:

Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Thorpe, 227 USPQ 964, 966; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 2113.

Claims 17 and 18 do not distinguish over the Hofmann reference regardless of the process used to form the vertical channel, because only the final product is relevant, and not the process of making such as epitaxial deposition.

14. In reference to claim 19, Hofmann (USPN 5,998,261) discloses a similar device. Figure 5 of Hofmann illustrates a memory device with a buried source (14a) formed over a substrate (1). It is understood that a vertical channel is formed over the buried source (14a). A drain (14b) is over the vertical channel. A floating gate (11) is formed over the substrate (1). A select gate (13), in a trench in the substrate (1), is perpendicular to the floating gate (11). Figure 6 also shows this situation. The memory cell area is  $2F^2$  (column 6, lines 15-19); which is less than  $4F^2$ .

15. With regard to claim 22, Hofmann (USPN 5,998,261) discloses a similar device. Figure 5 of Hofmann illustrates a memory device with a buried source (14a) formed over a substrate (1) having at least one semiconductor layer. It is understood that a vertical channel is formed over the buried source (14a). A drain (14b) is over the vertical channel. There is a tunnel oxide layer (10) formed over or above the drain (14b). A floating gate (11) is formed over the tunnel oxide

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layer (10). A select gate (13), in a trench in the substrate (1), is along the sidewalls of the trench. Figure 6 also shows this situation. The memory cell area is  $2F^2$  (column 6, lines 15-19); which is less than  $4F^2$ . The examiner notes that the applicant has also claimed that the floating gate is "self aligned." The applicant has defined a "self-aligned gate" to mean that the gate electrodes are formed before the source and the drain (p. 19 of the specification, lines 11-13). This language places claim 22 into the form of a product-by-process claim:

Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Thorpe, 227 USPQ 964, 966; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 2113.

Claim 22 does not distinguish over the Hofmann reference regardless of the process used to form the floating gate, because only the final product is relevant, and not the process of making such as forming the gate electrodes before the source and the drain.

16. With regard to claim 26, Hofmann (USPN 5,998,261) discloses a similar device. Figure 5 of Hofmann illustrates a memory device with a first n-type layer (14a) or source, formed over a substrate (1). There is a p-type layer (3) over a first n-type layer (14a). There is a second n-type layer (14b) or drain, formed in the p-type layer (3). There is a substantially vertical select gate (13) formed in a select trench. The memory cell area is  $2F^2$  (column 6, lines 15-19); which is less than  $4.5F^2$ .

17. In reference to claim 27, there is a tunnel oxide layer (10) formed over the substrate (1).

18. With regard to claim 28, there are wordlines (13) formed over the substrate. Although not seen in the figures, it is understood that digitlines or bitlines, are over the substrate and are connected to at least one of the n-type layers (14a, 14b).

***Double Patenting***

19. Applicant is advised that should claim 17 be found allowable, claim 18 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

***Allowable Subject Matter***

20. Claims 1-9, 15, 16, 20, 21, 24, 25, and 29-33 are allowed.

21. The following is a statement of reasons for the indication of allowable subject matter: the examiner is unaware of any non-volatile memory cell having an area of  $2F^2$  which has a control or select gate in a trench, the source at the bottom of the trench, a drain at the top of the trench, and a horizontal floating gate over the drain.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (703) 306-5688. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the


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organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

KVQ

December 10, 2002

  
NATHAN J. FLYNN  
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